European Commission

25 APRIL, 2018

plaCMOS

***plaCMOS* is developing a technology that will allow a massive increase in the speed of optical transceivers used in datacenters. Combining innovations in materials, devices and integration concepts, *plaCMOS* will yield a super-fast, micrometer-scale optical engine capable of transmitting and receiving data at world's fastest speed of 200 Gbit/s per optical channel**

AT A GLANCE

Project title:
Wafer-scale, CMOS integration of photonics, plasmonics and electronics for mass manufacturing 200Gb/s NRZ transceivers towards low-cost Terabit connectivity in Data Centers.

Project coordinator
Mellanox Technologies, Israel

Partners from:
Mellanox (IL), Micram (DE), IHP - Innovations for High Performance Microelectronics (DE), IBM Research Zurich (CH), Universitaet des Saarlandes (DE), ETH Zurich (CH), Aristotle University of Thessaloniki (GR)

Duration:
12/2017 – 11/2020

Total cost:
4.04 M€

Programme:
H2020-ICT-2017-1

Further information:
www.placmos.eu

Challenge

The tremendous growth of photonic integration technology is paving the way for ICT services to scale faster over the coming years. This relentless growth of data traffic raises the need for ultra high speed network transmission especially within the data centers. To meet the surging bandwidth requirements, data centers push the research towards short-reach optical interconnects operating at 100 Gb/s and beyond. There is an urgent need for faster, smaller and low-cost transceivers that will be capable of supporting data volume predictions and port densities of the upcoming decade. The technology that will allow a substantial leap in transceiver fundamental speed of an order of magnitude to what is currently available, while complying with wafer planar manufacturing will practically disrupt the global market.

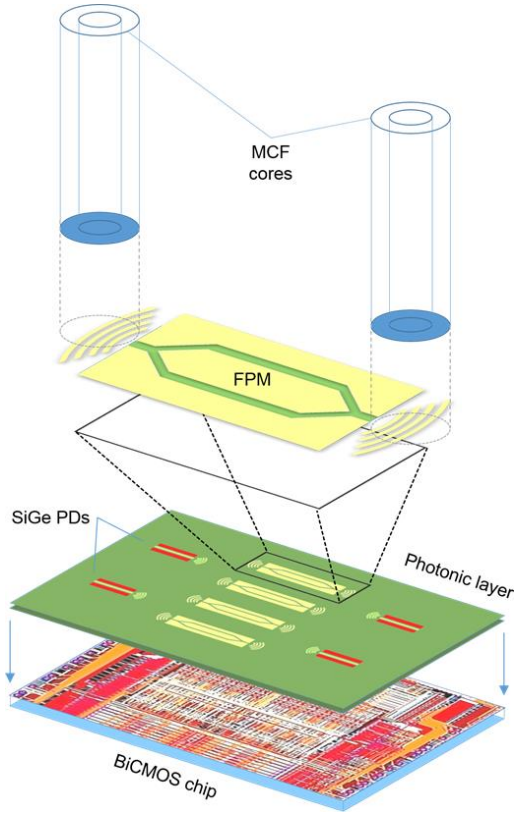
Concept

PlaCMOS will be based on the latest BiCMOS technology, and cointegrate it with a ferroelectric plasmonic modulator and a SiGe detector technology. Using ferroelectrics and SiGe, the device bandwidth will be enabled, yet using manufacturable concepts. By exploiting plasmonics rather than photonics *plaCMOS* will not only be able to extend

the bandwidth far beyond 100 GHz but also reduce the footprint of photonics to the micrometer scale.
While the project goes far beyond the current state-of-the art, the approach is not speculative but is substantiated by recent experiments performed by the members of the consortium that indicate that both electronic and photonic performance can be stretched beyond the current limits. To this end a team with complementary skillsets from both industry and academia – all with a track record in the field – have committed to reach ambitious objectives to demonstrate the technology.

Objectives

PlaCMOS's technology speed and scalability advantages will be validated in fully functional single channel and multi-channel (CWDM-based and SDM-based) transceiver prototype assemblies To demonstrate the technology, a single channel 200 Gb/s NRZ transmitter and receiver pair, and an ultra-compact 4×50 Gb/s transceiver directly interfacing a multicore fiber will be implemented. A CWDM variant of the 4×50 Gb/s transceiver will also be pursued. These will be enabled by the co-development of major advances in various fields. Novel ferroelectric thin film materials will be provided for thermally stable, high-speed modulators. *plaCMOS* will develop a novel type of modulator combining plasmonic waveguides with thin-film ferroelectrics exhibiting strong electro-optic effects. Novel broadband Germanium waveguide coupled photodetectors will be integrated with operation speed up to 200 Gb/s. A record high speed electronic IC platform will be developed to establish 200 Gb/s photonic modules in ultra-high speed integrated electro-optic engines. Finally, *plaCMOS* will anticipate future market needs by showing the integration process at a wafer scale, to combine world's fastest electronic and photonic active and passive components in ultra-fast, compact and low cost monolithic optical engines for future electro-optic transceivers.



Exploitation

To accelerate *plaCMOS* exploitation, a volume manufacturing and technology feasibility roadmap will be established, considering technical outcomes, market needs and application scenarios. *plaCMOS* will proactively prepare the ground for the market adaptation of its PIC technology by conducting techno-economic studies versus predominant application scenarios and technology forecasts for the PIC platform as well as for the transceiver modules. *plaCMOS* will use system-level simulation tools and pilot validation outcomes to project and optimize *plaCMOS* competencies in different hierarchy levels of optical interconnect (inter-data center, intra-data center, rack-to-rack etc.) for mega-data centers and future HPC applications. Finally, the broad application potential of *plaCMOS* PIC technology will be addressed by exploring novel functionalities in non-volatile ferro-electric switches.

For further information:

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